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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/529,465

03/28/2005

Nobuhiro Suzuki

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8284

26021 7590 05/30/2007

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EXAMINER

SMOOT, STEPHEN W

ART UNIT

PAPER NUMBER

2813

MAIL DATE

DELIVERY MODE

05/30/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,465	SUZUKI ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 March 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3-28-05; 8-15-05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to application papers filed on 28 March 2005, which includes a preliminary amendment that has been entered.

Drawings

1. Figs. 12-20 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see page 1, line 14 to page 2, line 9 and page 4, line 27 to page 5, line 13). See MPEP § 608.02(g).

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Semiconductor Integrated Circuit Device that Includes External Wiring Formed Around a Side Surface of a Semiconductor Chip with a Protection Film Covering an End of the External Wiring.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (US 2002/0047210 A1 – from applicant's IDS filed on 3-28-05).

Referring to Figs. 44-46 and paragraphs [0335] to [0363], Yamada et al. disclose a thirteenth embodiment that includes the following process steps:

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- Elements (not shown) corresponding to individual semiconductor chips are formed on a multi-chip substrate (212) that is partitioned with a scribe line (216) (see Fig. 44A and paragraphs [0335] to [0337]);
- Internal wiring (219, 220, 221) is then formed extending across the scribe line (216) and is electrically connected to surface electrodes (213) corresponding to adjacent semiconductor chips as shown in Fig. 44F;
- A bevel (i.e. a groove) is then cut along the scribe line (216) from the rear surface of the substrate (212) to expose the internal wiring (221) (see Figs. 44B, 45B and paragraph [0345]);
- A layered metal film (230, 231) is then formed on the entire rear surface of the substrate and also covers the beveled region as shown in Fig. 45D and as described in paragraph [0350];
- A plating resist (233) is then used to selectively grow conductive patterns (232), which in turn are used to pattern the layered metal film (230, 231) by removing it from the bottom portion of the bevel to thereby define external wirings (230, 231, 232) (see Figs. 46A, 46B and paragraphs [0351] to [0352]);
- The external wirings (230, 231, 232) are then covered by blanket depositing an insulating layer (235) (i.e. a protection film), which is subsequently patterned with a mask to expose the bottom portion of the bevel and to define electrode openings (234) as shown in Fig. 46C and as described in paragraph [0353];
- The substrate is then separated into individual semiconductor chips along the scribe line as shown in Fig. 46D; and

- The separation width corresponding to the scribe line is narrower than either the width of the bevel or the width separating the external wirings (230, 231, 232) that is defined by the plating resist (233) because the separation width is narrowed by twice the thickness of the insulating layer (235) as shown in Figs. 46C, 46D.

These are all of the process limitations as set forth in claim 1-3 of the applicant's invention.

Regarding the structure as claimed in claims 4-5, Fig. 46D shows semiconductor chips with these features. Namely, a semiconductor substrate (212) with elements (not shown), internal wiring (221 in Fig. 46A) that extends to the chip periphery, external wiring (232 in Fig. 46B) detouring around a side surface of the substrate (212) and electrically connected to the internal wiring (221 in Fig. 46a), and the sides of the external wiring (232 in Fig. 46B) are covered by the insulating layer (235 in Fig. 46C) which further has an outermost surface that defines side surfaces of the semiconductor chips.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 2002/0047210 A1 – from applicant's IDS filed on 3-28-05) as applied to claim 4 above, and further in view of Wolf and Tauber.

As shown above, Yamada et al. anticipate claim 4 of the applicant's invention. However, although Yamada et al. teach that both the internal wiring and the external wiring can be aluminum (see paragraphs [0340] and [0351]), they do not expressly teach or suggest that the aluminum can include copper as an additive, which is a requirement of claim 6 (for the external wiring) and of claim 7 (for the internal wiring). Wolf and Tauber teach that aluminum thin films containing small quantities of copper additive are known to the semiconductor art (see sentence bridging pages 333-334).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Yamada et al. with those of Wolf and Tauber in order to use aluminum with copper additive, as taught by Wolf and Tauber, for both the internal wiring and the external wiring material. Wolf and Tauber recognize that the addition of small amounts of copper to aluminum thin films improves electromigration resistance and reduces the propensity of hillocks from forming on the aluminum surface (see sentence bridging pages 333-334).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prabhu et al., Ference et al., MacIntyre, and Bolam et al. teach integrated circuit packaging methods.

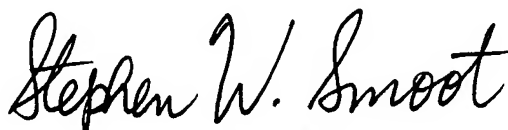
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on Monday to Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWS

A handwritten signature in black ink that reads "Stephen W. Smoot". The signature is written in a cursive, flowing style.

**STEPHEN W. SMOOT
PRIMARY EXAMINER**